Automotive Chiplets in the Era of AI

Dr. Éricles Sousa
SoC Architect and UCIe Automotive WG Co-Chair
December 3, 2024

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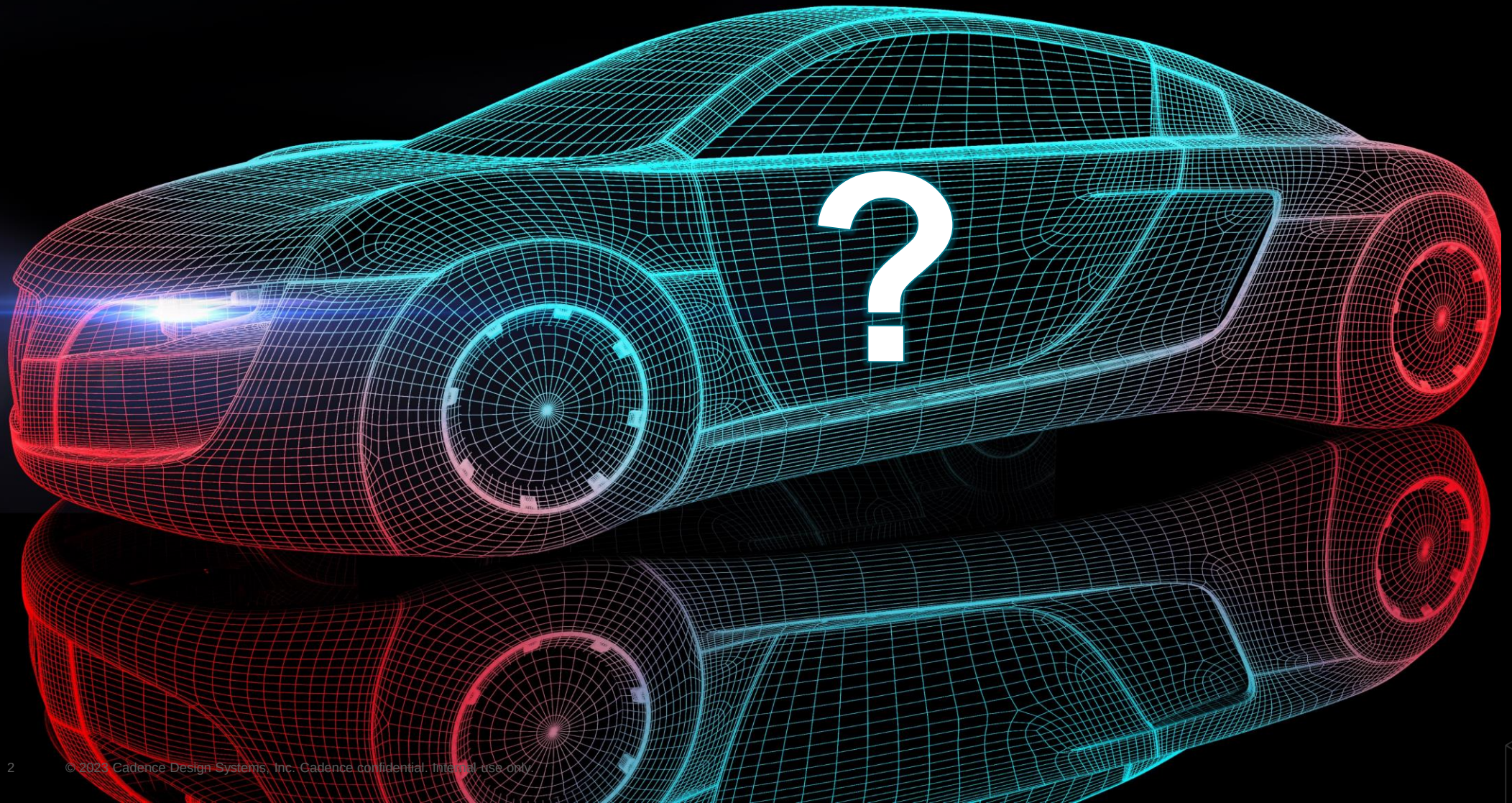
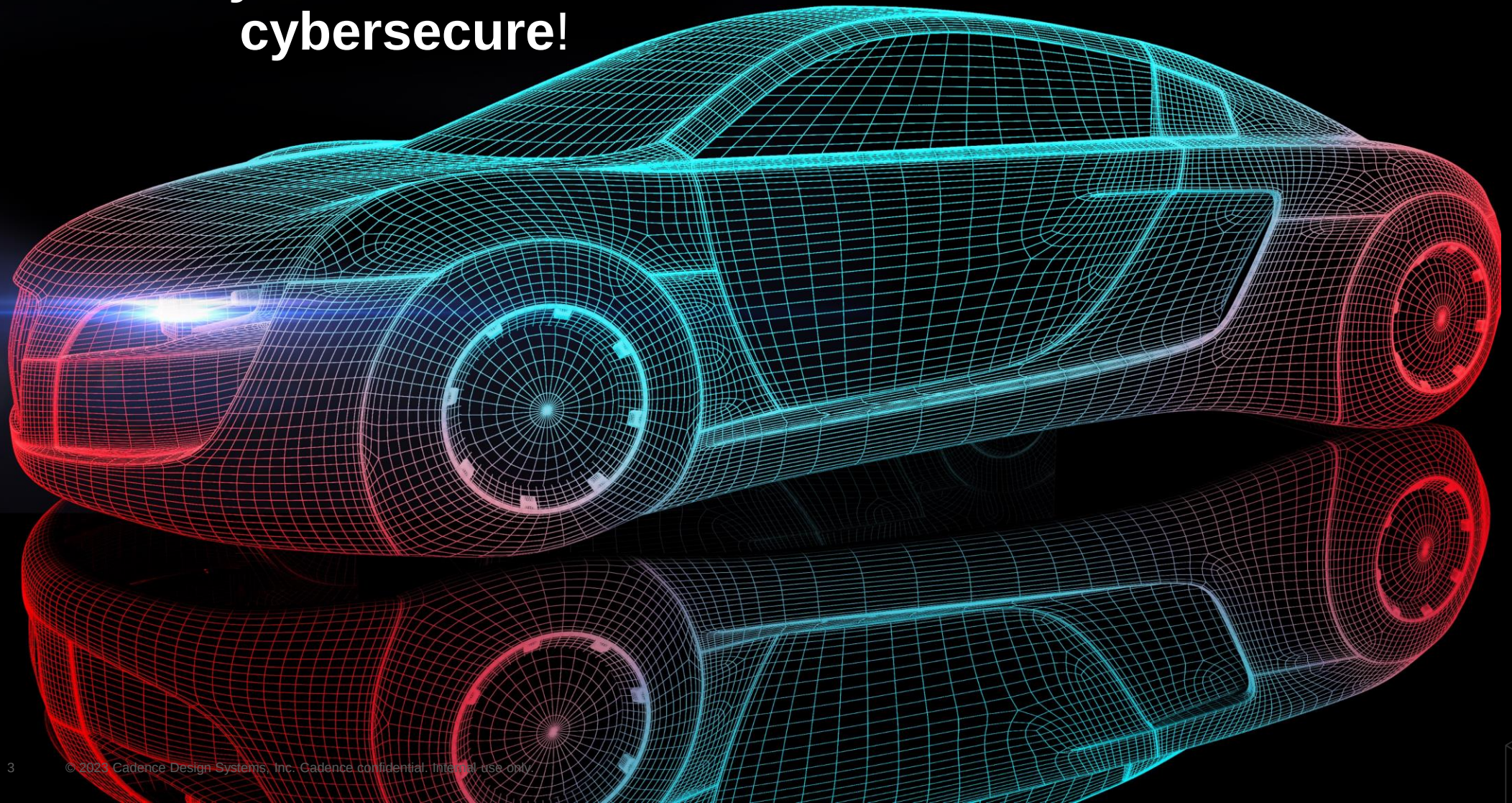
What will cars of the future be like?



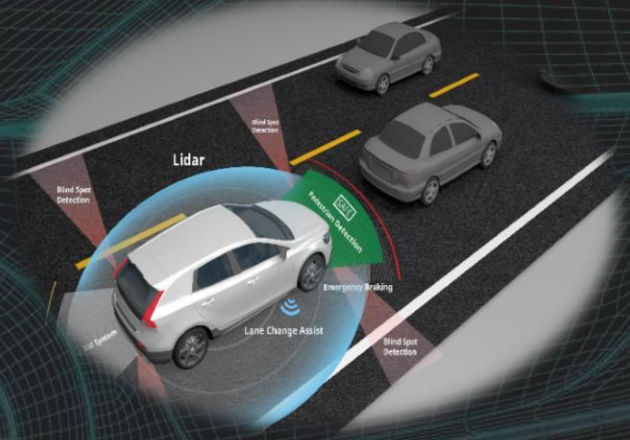
The car of the future will be **autonomous**, **safer**, **all-electric**, **fully connected**, and **cybersecure**!



The 5 Must-Have Features of Modern Automotive SoCs

The car of the future will be autonomous, safer, all electric, fully connected, and cybersecure!

Real-Time and
High-Performance Computing



Safety

Low-power consumption

AI-driven Connectivity

Cybersecurity

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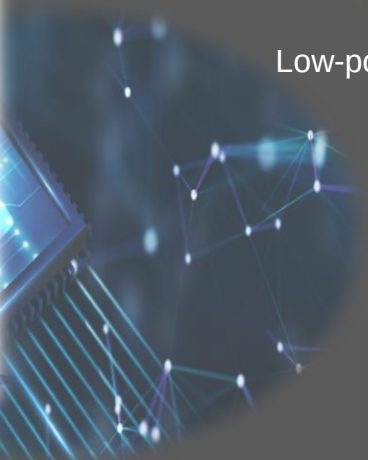


Cybersecurity

Outline

Disaggregation: The benefits of Chiplets

UCIe Standard

Key Challenges in Automotive Chiplet-based SoC

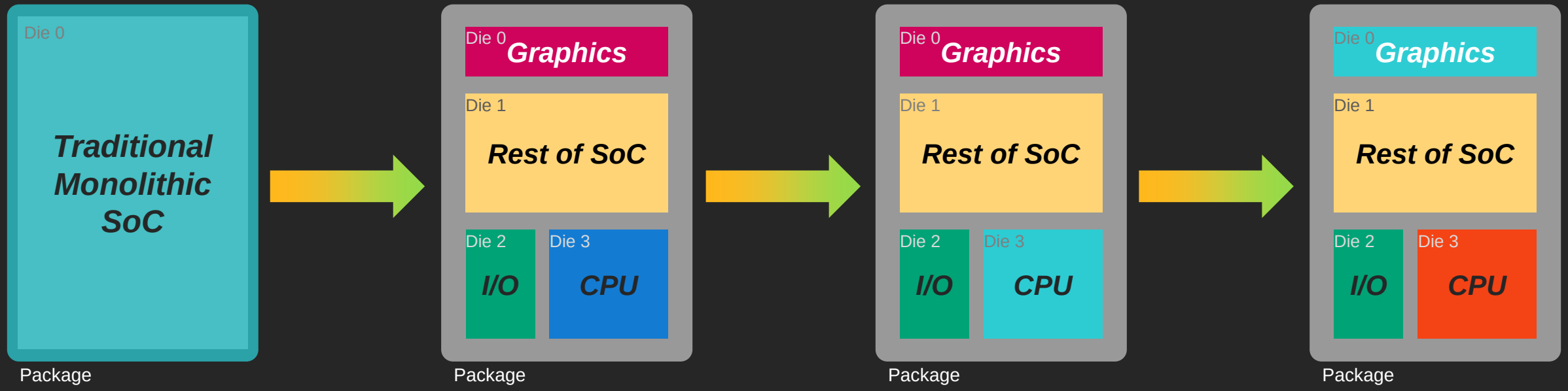
Examples

Summary

Disaggregation

The Benefits of Chiplets

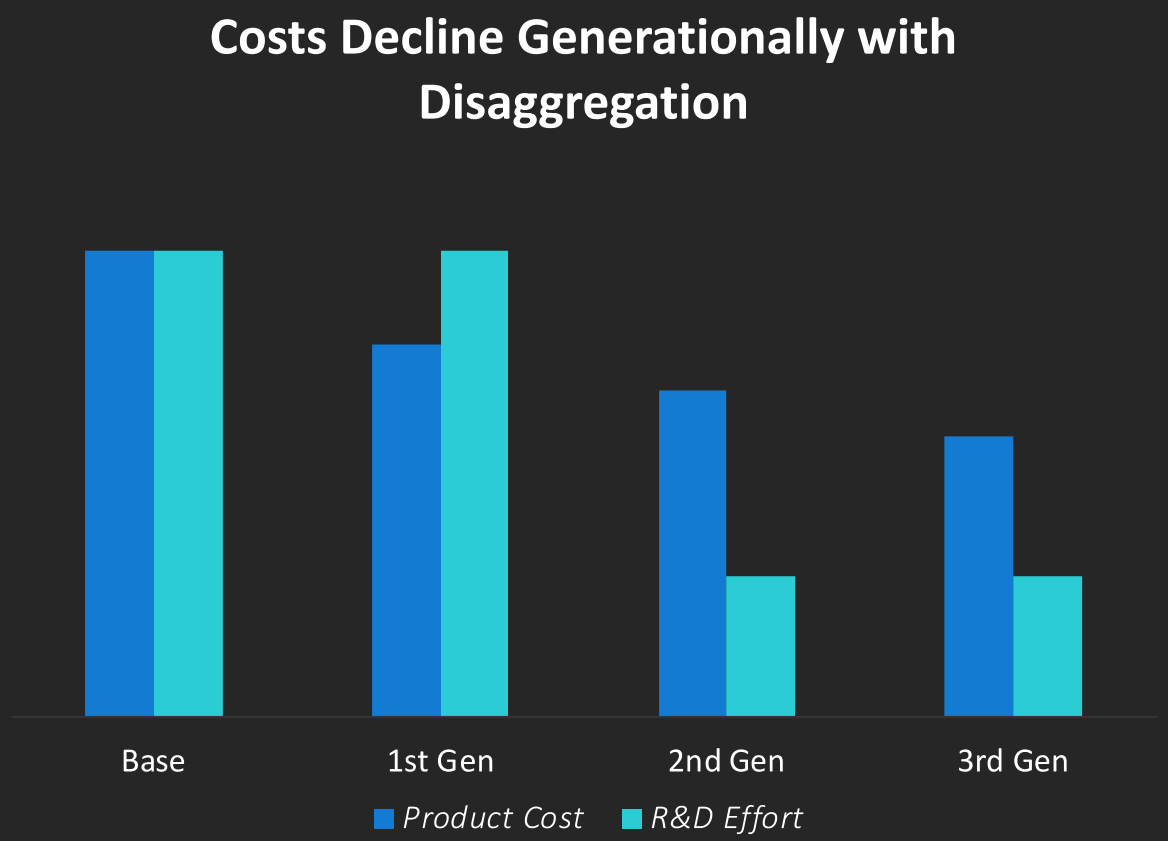
Disaggregation – An example

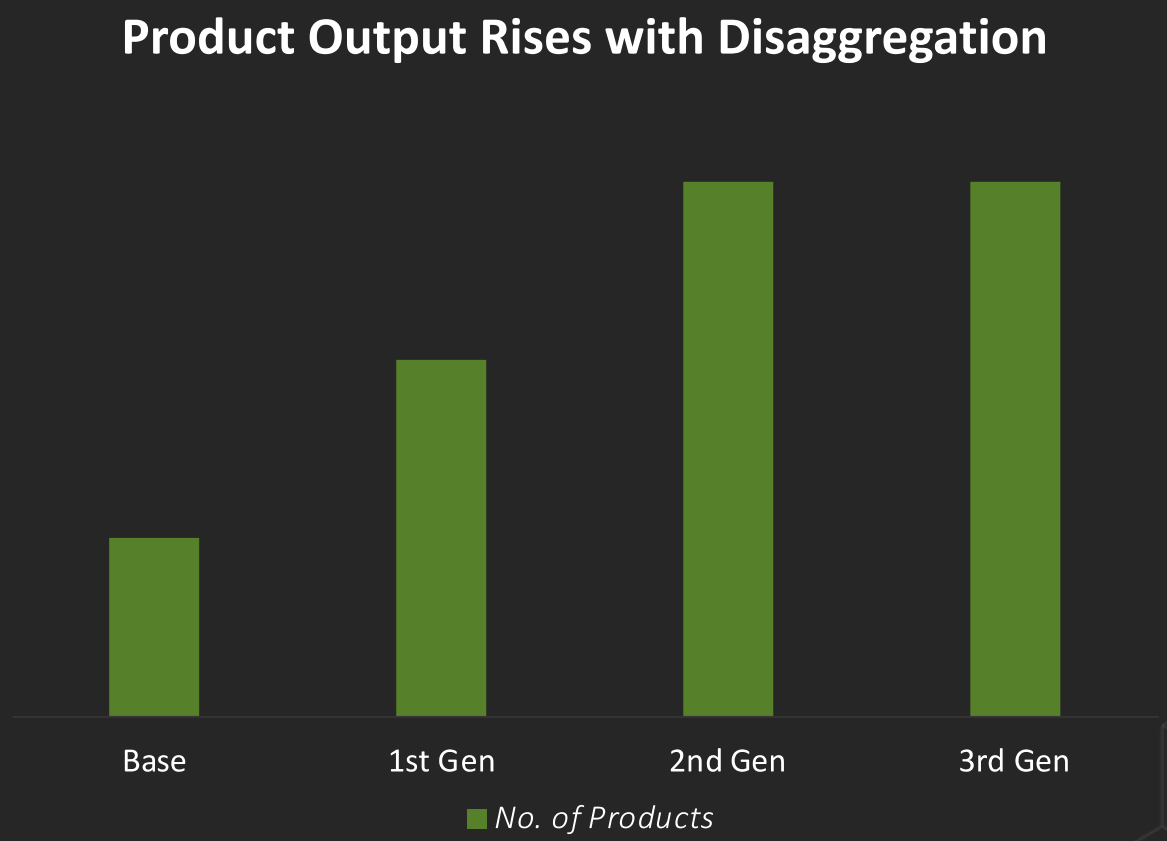


- DDR5
- Processor Cores
- NPU
- GPU
- PCIe, Ethernet
- Power Management
- Bus, Network-on-chip, etc.

Disaggregated designs enabling multi-die package modules

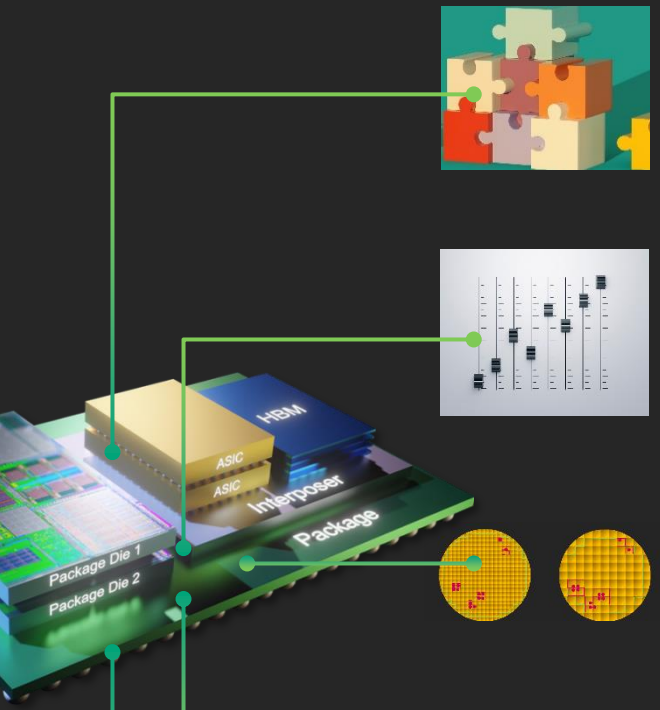
Impact on Cost (Capex/Opex) and Output





Source: Phelps, B. Disaggregated Designs and Chiplets – Addressing SoC and Processor Designs in the AI era. Cadence Distinguished Speaker Series, April 2024.

The Advantage of Chiplets (Disaggregated Design)

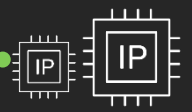


Modularity – Create complex systems with pre-designed, pre-verified chiplets instead of monolithic chips

Customization – Combine different chiplets in various configurations to meet specific performance/power/cost needs

Improved Yield on advanced complex nodes

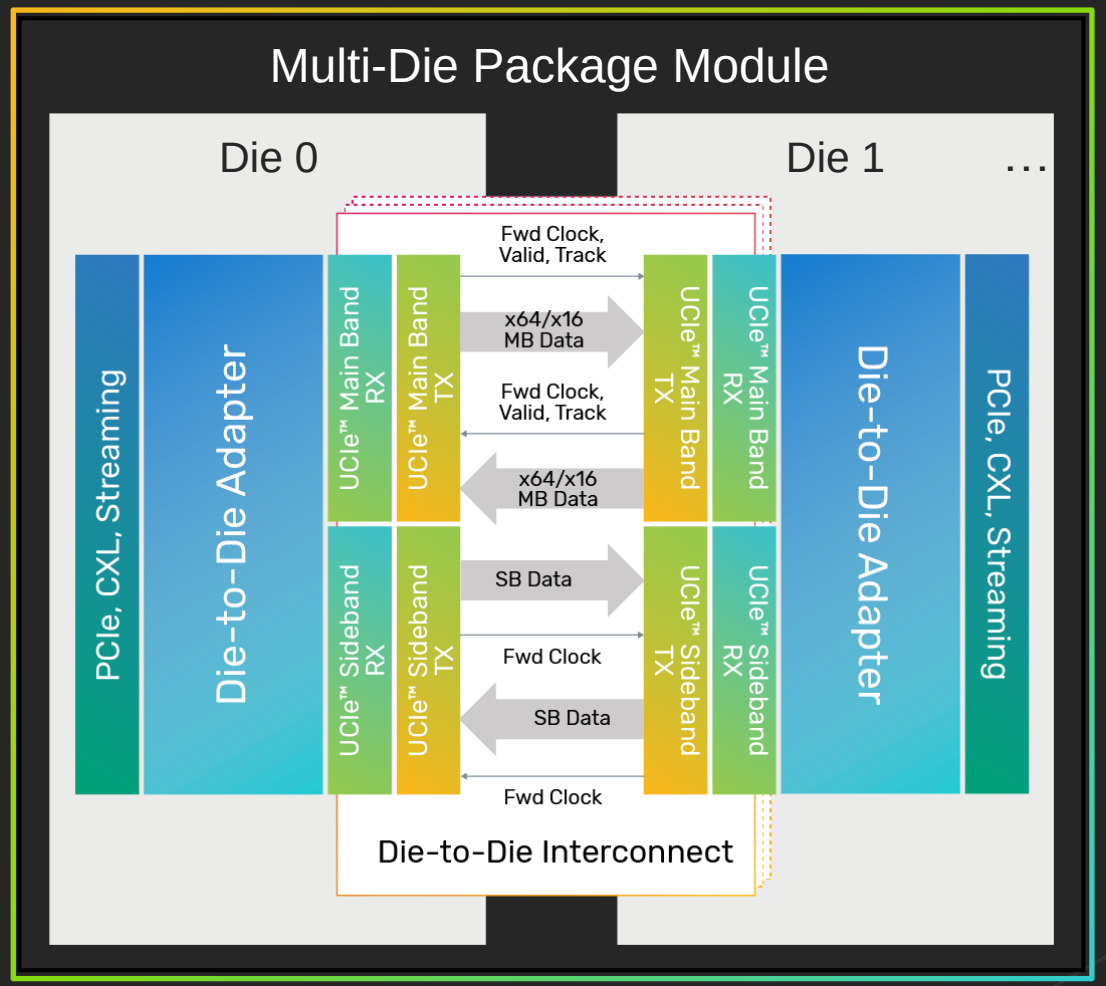
Improved PPA – Fitting the right IP to the right process

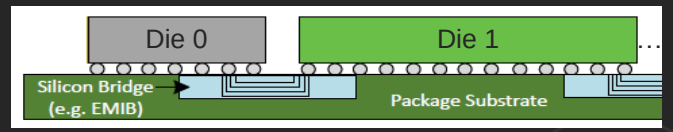


Improved Scalability – New chiplets developed/integrated into existing designs to improve performance/add features without redesigning entire chip

Chiplets – Scalable Multi-Die Heterogeneous Integration

- Enables multi-die system in package integration for high-performance computing (incl. AI/ML)
- Together with AI, Chiplet has been considered **1 of the 10 Breakthrough Technologies** in 2024 (Source: MIT Tech Review)
- UCIe™ is the Universal Chiplet Interconnect Express, a type of die-to-die (D2D) interconnect





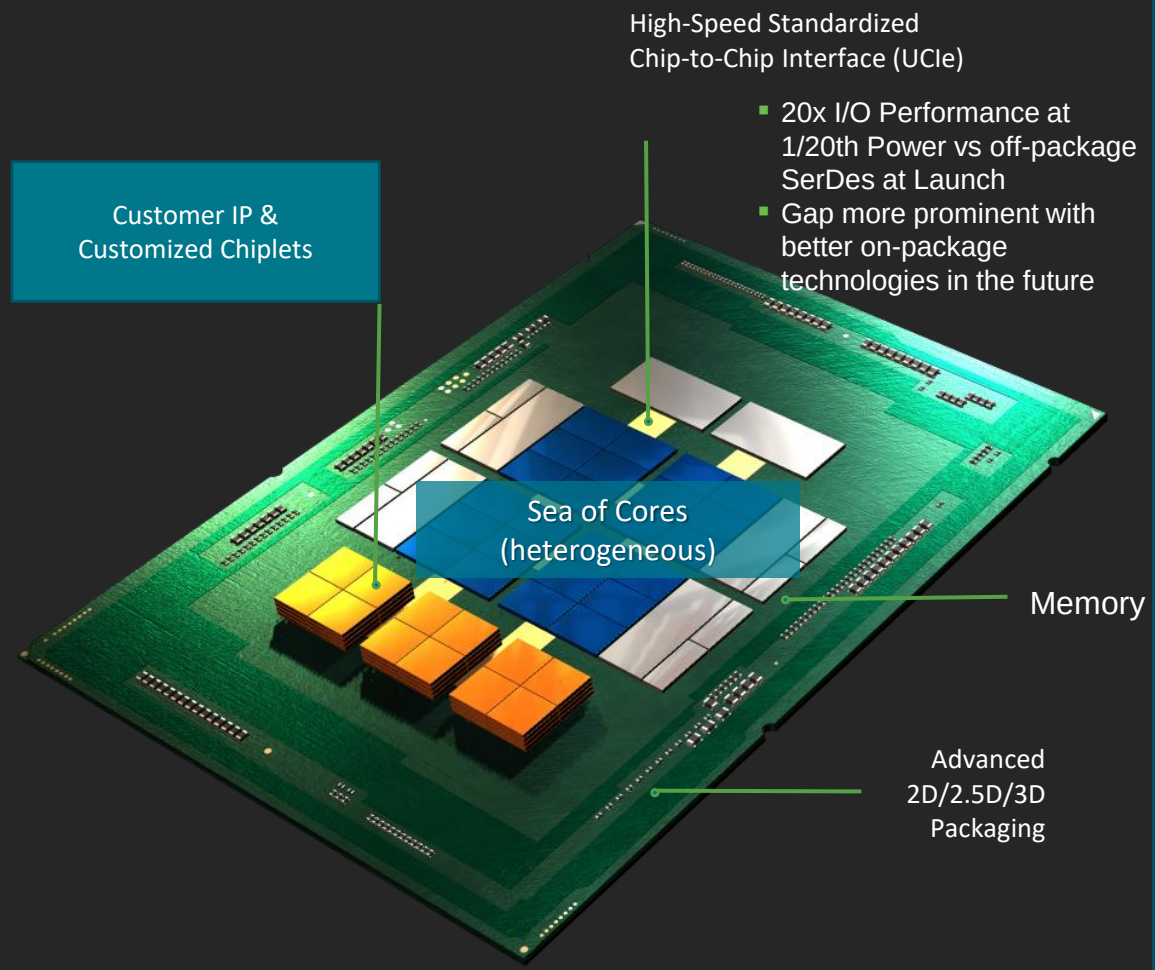
Universal Chiplet Interconnect Express (UCIe) Consortium

Universal Chiplet™ Interconnect Express

cadence®

Motivation

OPEN CHIPLET: PLATFORM ON A PACKAGE



Heterogeneous Integration Fueled by an Open Chiplet Ecosystem
(Mix-and-match chiplets from different process nodes/fabs/companies/assembly).

Align the Industry around an open platform to enable chiplet-based solutions

- Enables construction of SoCs that exceed maximum reticle size
  - Package becomes new System-on-a-Chip (SoC) with same dies (Scale Up)
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
  - Enables optimal process technologies
  - Smaller (better yield)
  - Reduces IP porting costs
  - Lowers product SKU cost
- Enables a customizable, standard-based product for specific use cases
- Scales innovation

Universal Chiplet Interconnect Express

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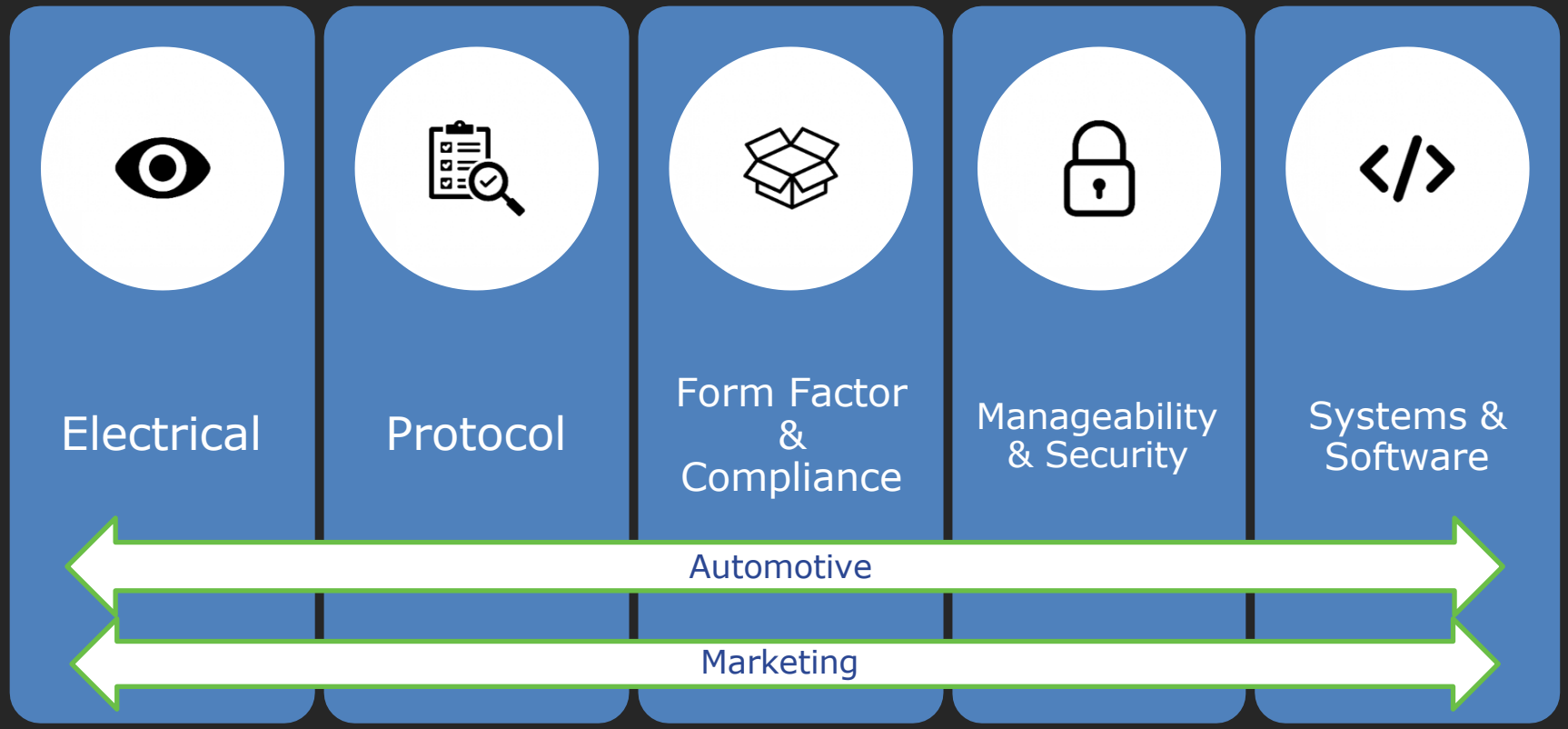
UCIe Consortium Working Groups

Working Groups are identifying and addressing the demands of a complete, full-stack solution for strengthening the open standards-based ecosystem.

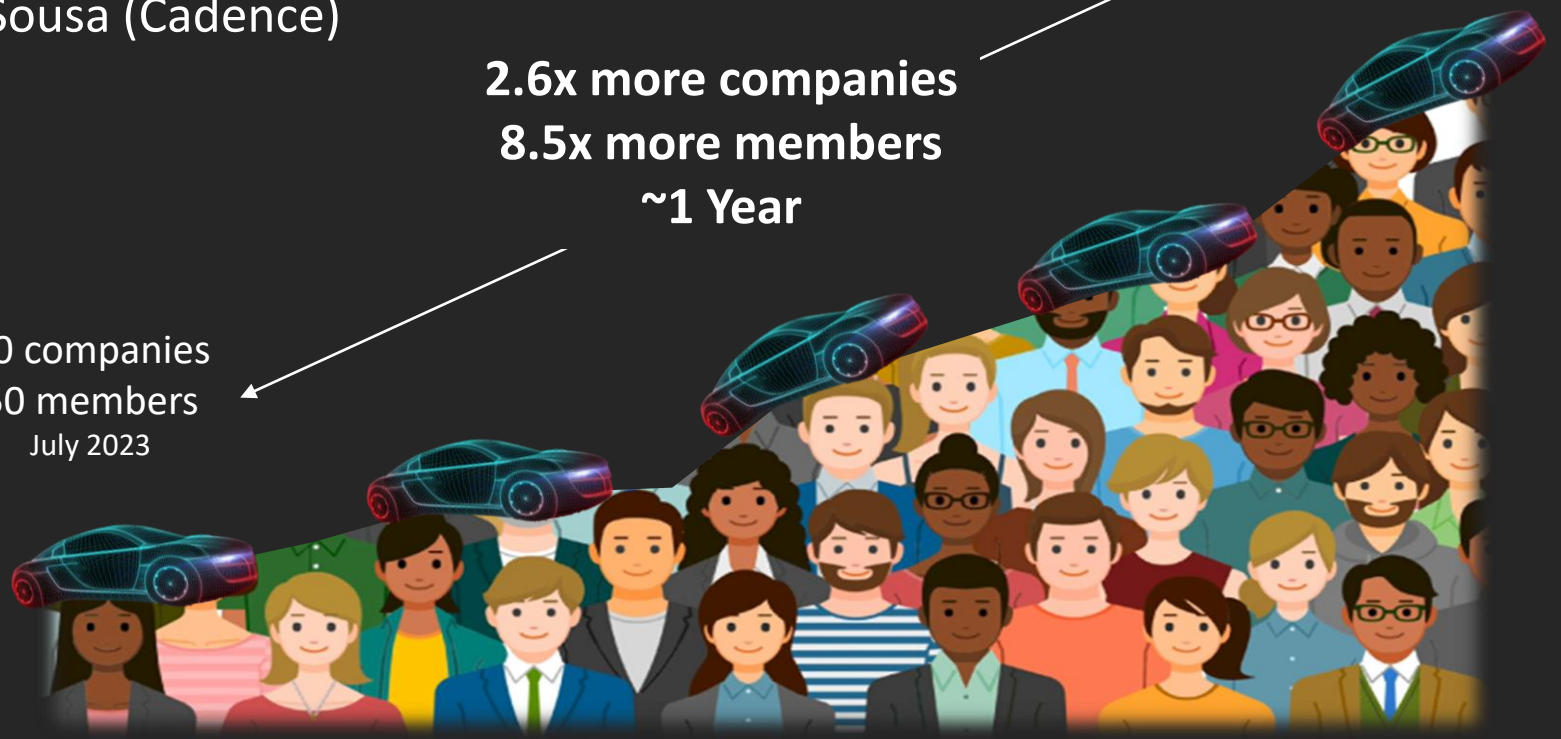


The Automotive WG in Numbers

Become a member

As Co-Chair of the UCIe Automotive WG, Cadence reiterates its commitment to leading the development of chiplets in the automotive industry.

- Co-Chairs:
  - Bala Chavali (AMD)
  - Dr. Ericles Sousa (Cadence)



Universal Chiplet Interconnect Express

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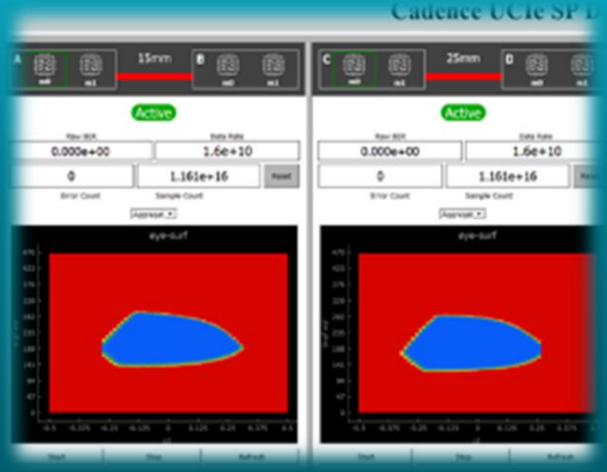
Automotive Challenges

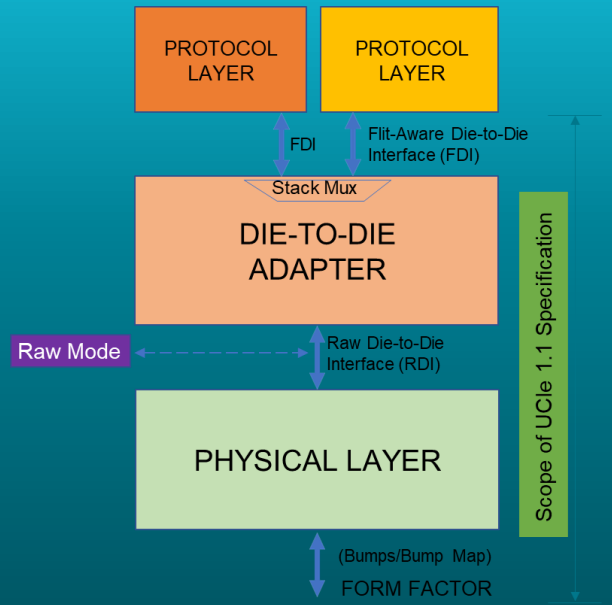
UCIe Specification

Key Challenges in Automotive and UCIe Enhancements

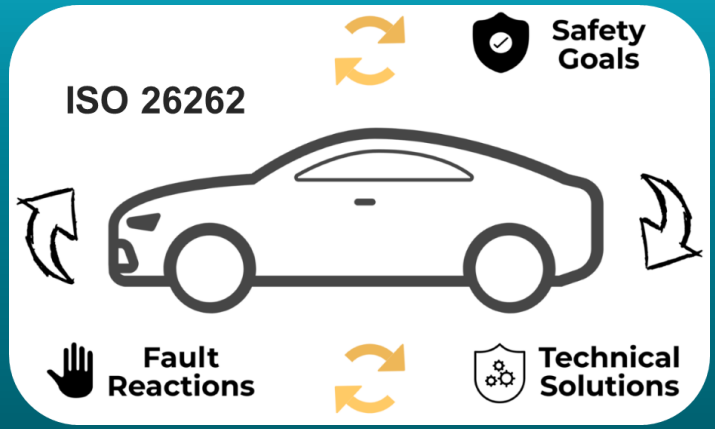
Link Health Monitoring



Interoperability



Functional Safety



Universal Chiplet Interconnect Express

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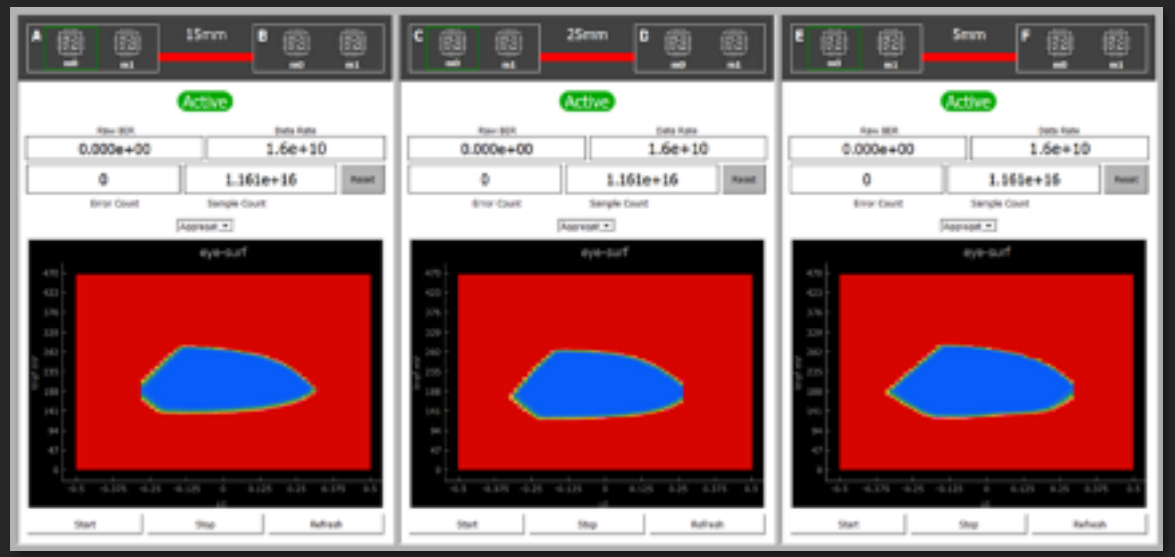
UCIe 1.1: Automotive Enhancements

Link health monitoring

- Preventive Monitoring:
  - Added new registers to capture Eye Margin
  - SW can trigger periodic retrain of the link to get eye margin information

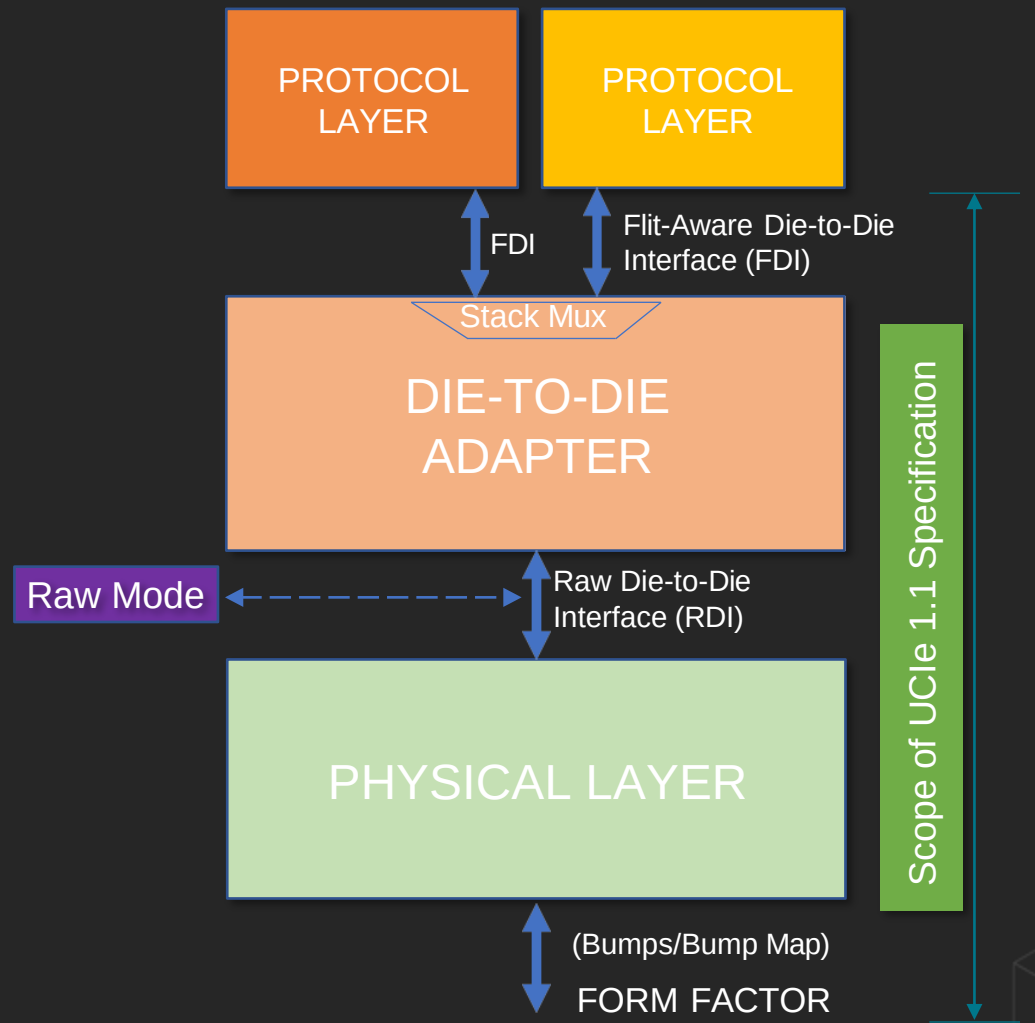


- Run-Time Testability of Link Health
  - Enhancements in UCIe 1.1: Per-Lane error Log/counter with the ability to send an interrupt
  - Usage: Software can inject periodic parity Flit and monitor the UCIe 1.1 error log

UCIe 1.1: Automotive Enhancements

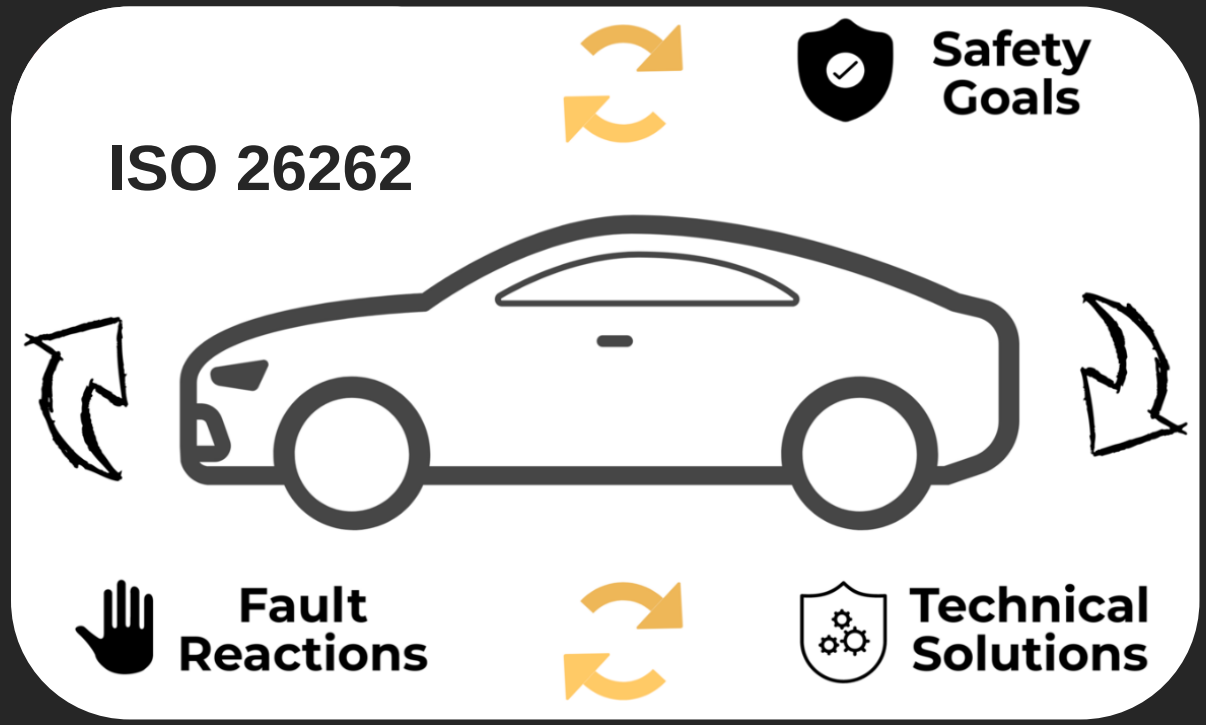
Interoperability and multiprotocol support

- UCIe™ 1.1 supports
  - PCIe,
  - CXL,
  - Streaming Protocols
    - AXI, CHI, SMP coherency protocols, etc.
- Streaming Protocols can use the D2D adapter
  - Can be multiplexed with other protocols with on-demand interleaving



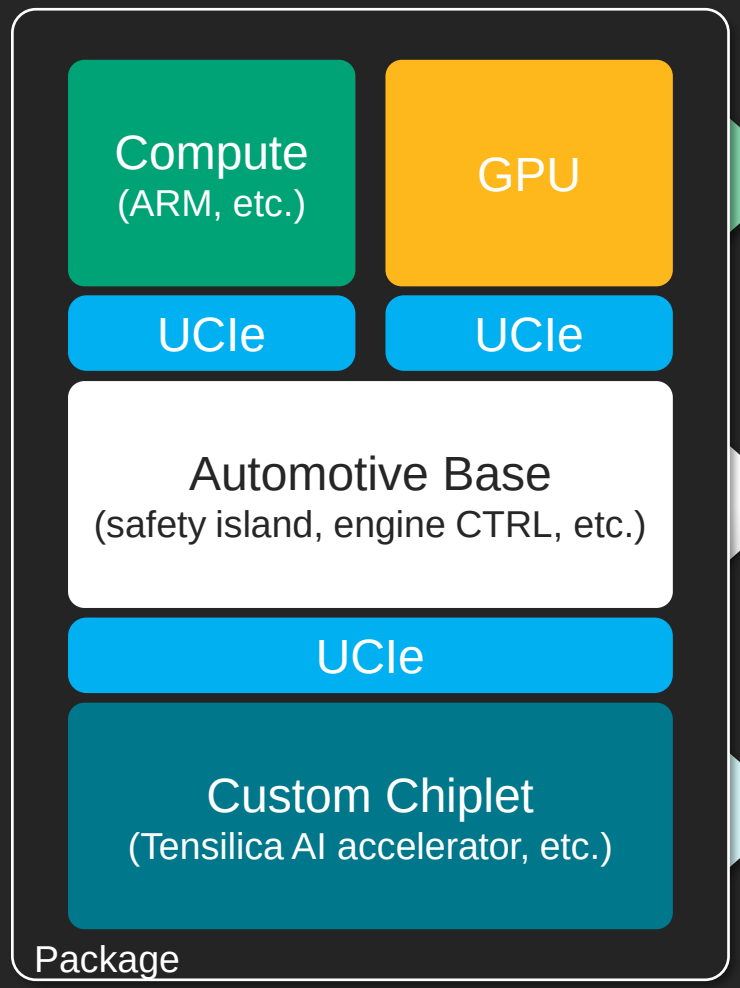
UCIe 1.1: Automotive Enhancements
Functional safety

- Main band:
  - CRC and Retry Mechanisms
- Sideband:
  - Data Parity and Control Parity provided for every sideband message
  - Parity errors on sideband are mapped to Uncorrectable Internal Errors
  - BER is 1e-27 or better at 800 MHz for both Standard and Advanced Packaging



Examples

A Generic Chiplet-based Architecture for Automotive

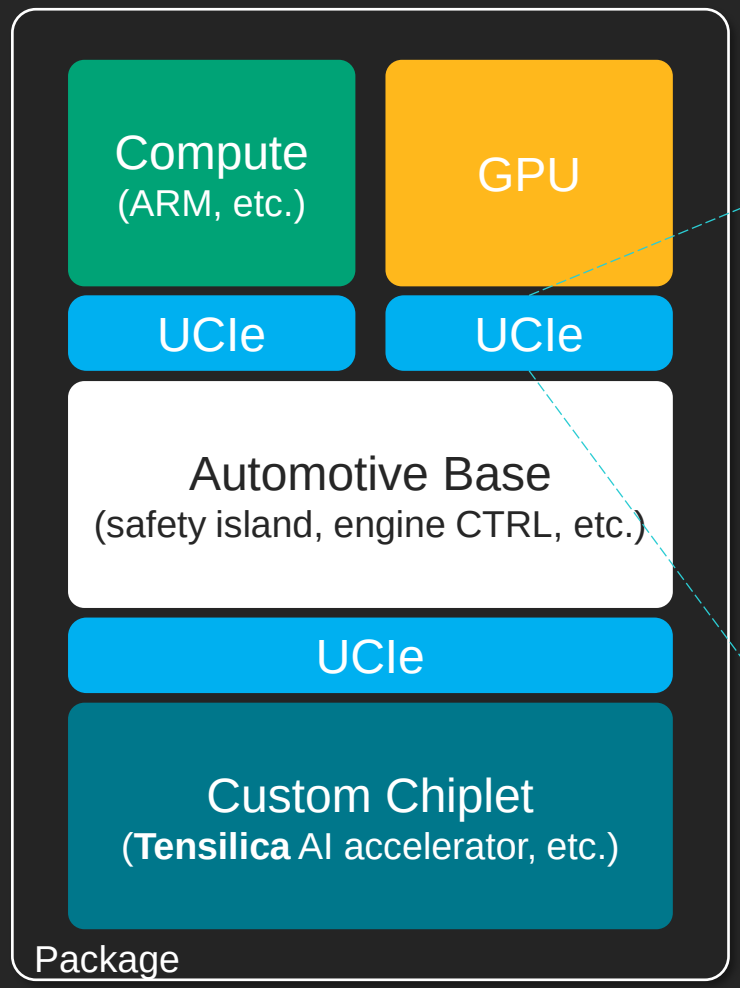


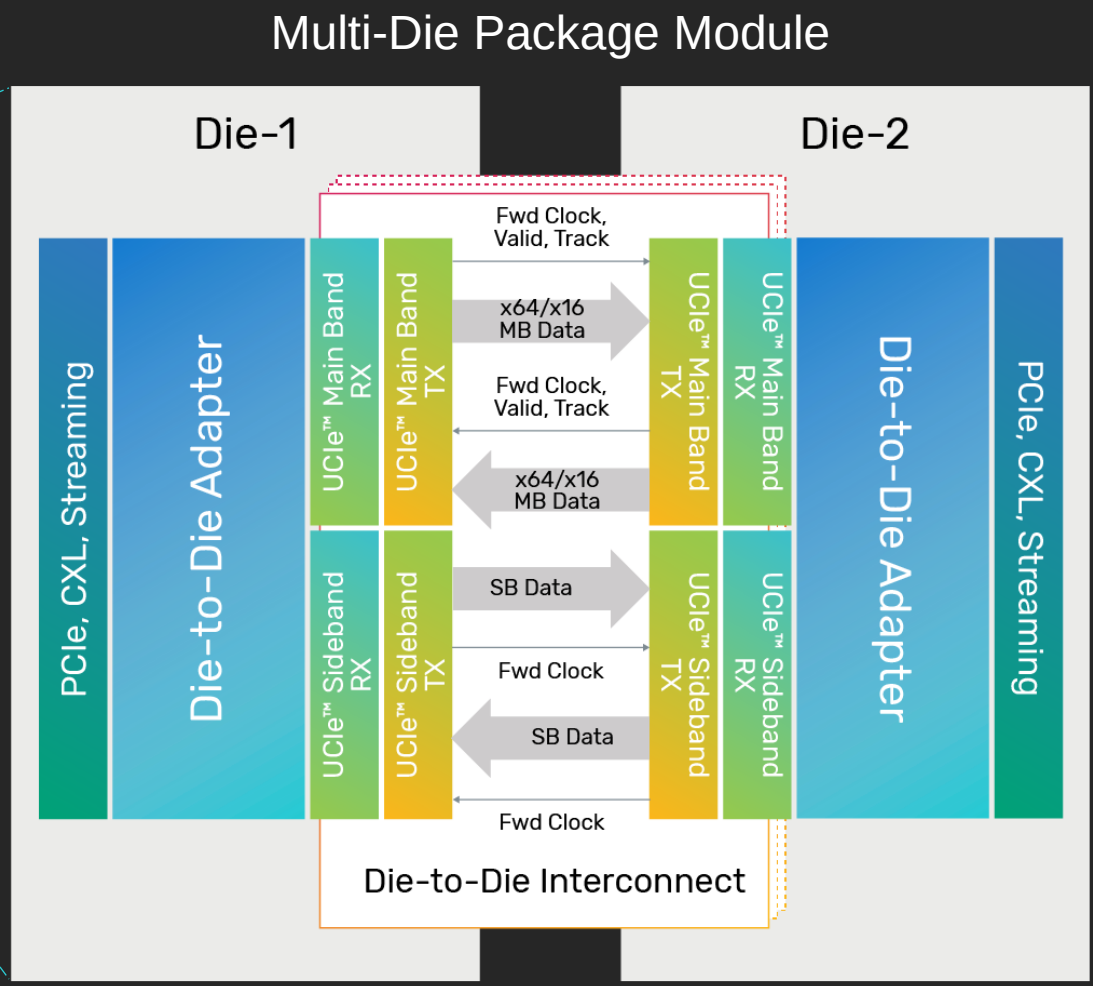
- Scalability and short innovation cycles
- Chiplets reuse ensuring functional scalability

- Compliant with the highest functional safety requirements
- Freedom from Interference
- Reliable for automotive use-cases

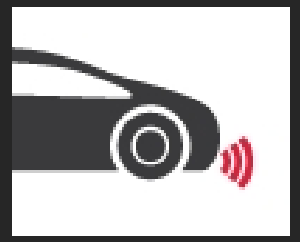
- Differentiation
- Demand for customization
- Inclusion of dedicated custom chiplets

A Generic Chiplet-based Architecture for Automotive



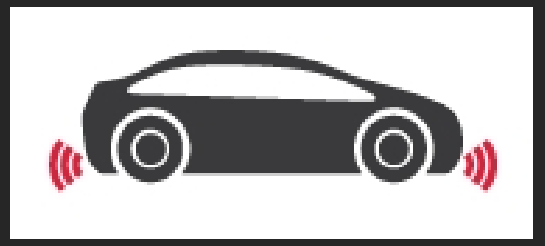


Scalable Multi-Core DSP and AI Platform



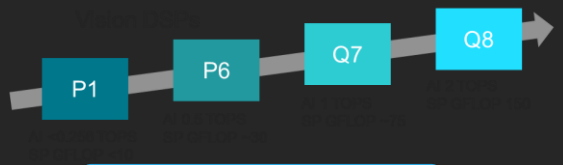
ADAS
0.25 – 4 TOPS

AI inference at the Edge



Autonomous Car
10s – 100s TOPS

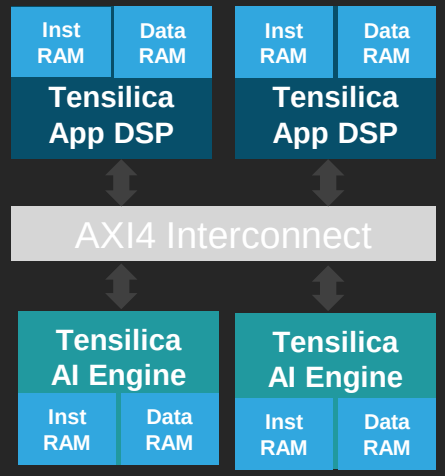
Tensilica DSPs



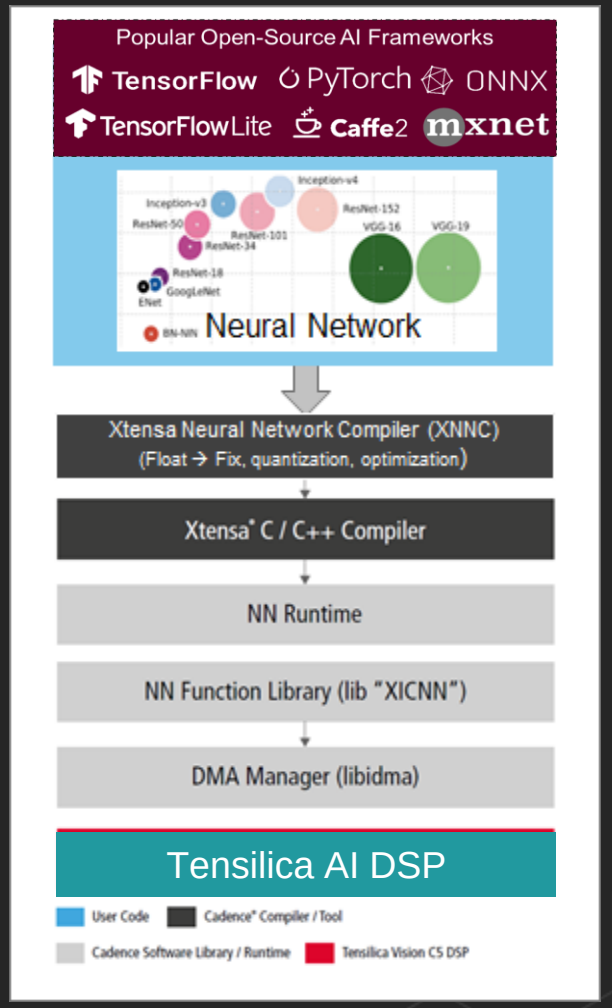
Tensilica® App DSP

Tensilica AI Engines

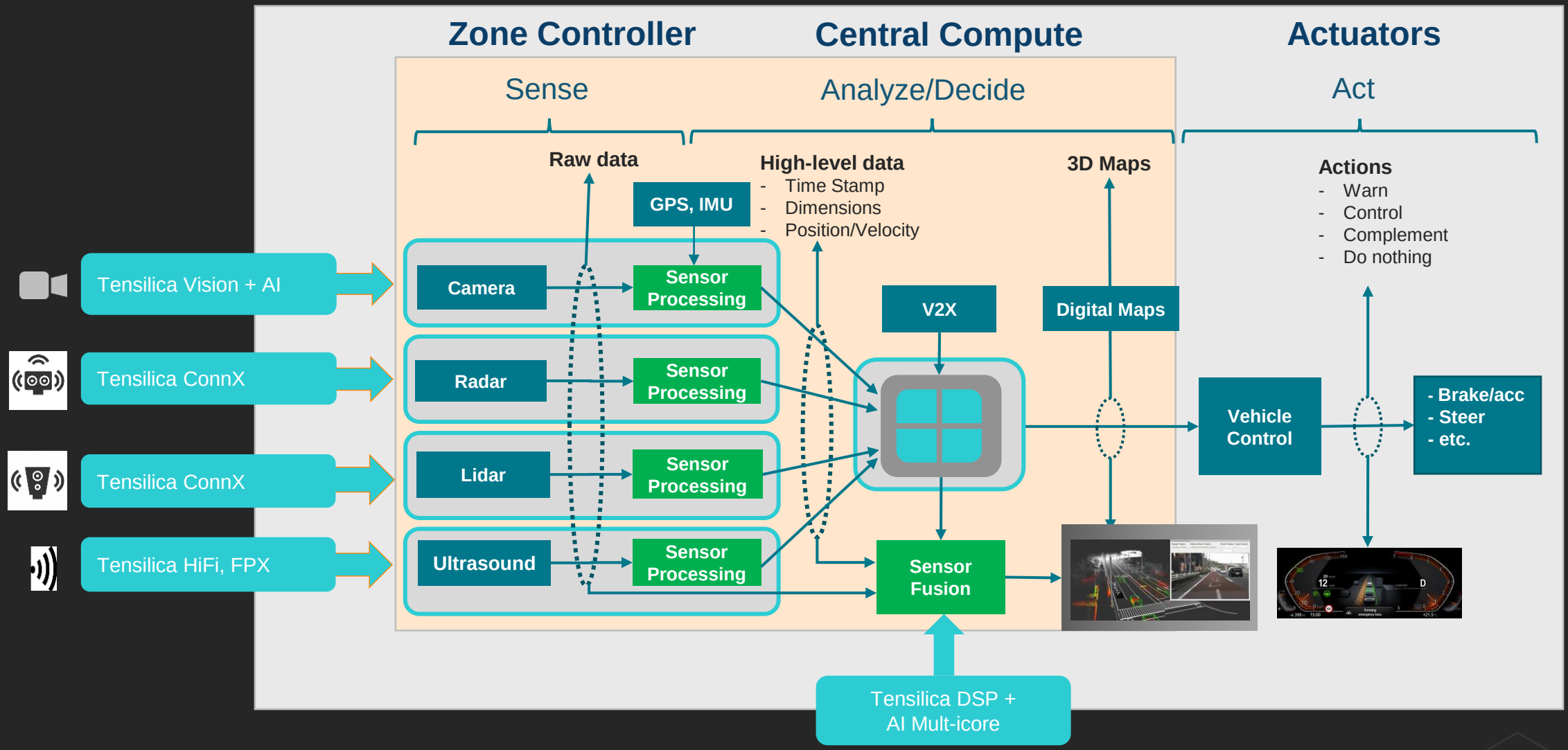
Scalable DSP Cluster



Automated AI Flow



Tensilica – a common hardware acceleration platform for ADAS



Tensilica – High Performance, Low Power Processing

Configurable Multi-Core DSP and AI Platform

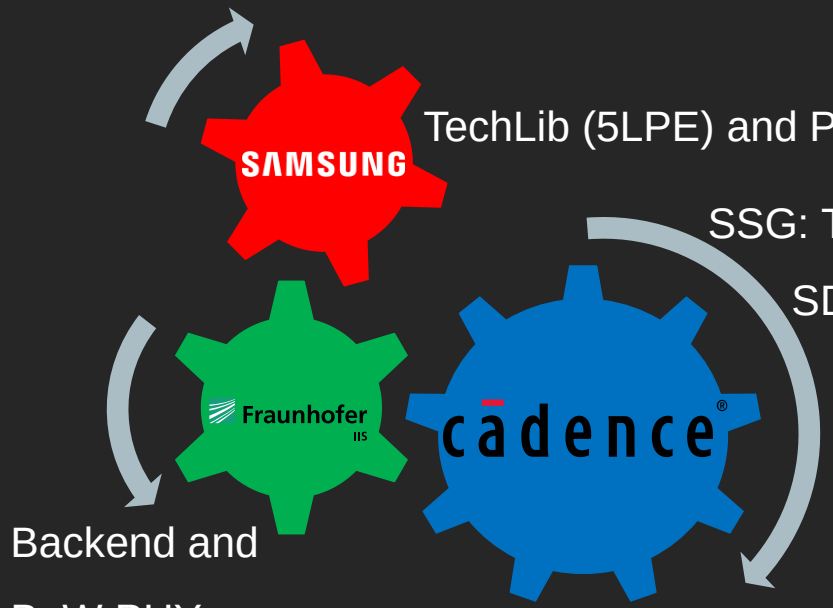
Audio/Voice	Radar/Lidar/Comms	Vision	FloatingPoint	AI Processor	Xtensa CPU
HiFi 5 (+ VFPU / NN)	**ConnX** B20, B10, BBE	**Vision** Q8, Q7	**FloatingPoint** KQ8, KQ7	**DNA** Multi-Core	**LX** Controller
HiFi HiFi 4, 3, 3z, 1	**Fusion** G6, G3, F1	**Vision** P6, P1	**FloatingPoint** KP6, KP1	**DNA** Single-Core	**NX** Controller

Xtensa®: The Configurable, Extensible Processor Platform

Custom ISA, Accelerators, Data Types, and Interfaces (TIE: Tensilica Instruction Extension)

Building a Chiplet Ecosystem

- Collaboration: Cadence, Samsung, and Fraunhofer



TechLib (5LPE) and PLL IP

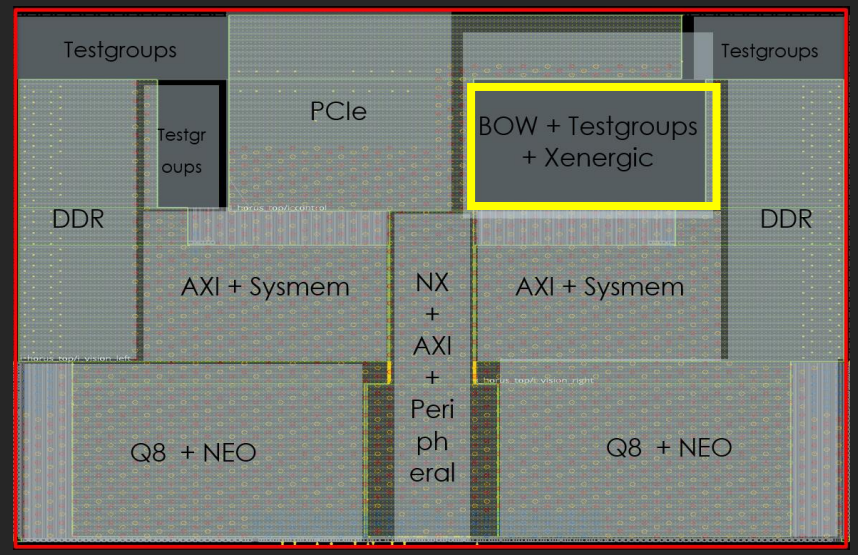
SSG: Tensilica, DDR, PCIe, etc.

SDE: Frontend design and verification.

To continue with Helium Digital Twin!

Backend and BoW PHY

Tapeout date: June 2024
BoW Chiplet Platform



BoW - Bunch of Wires

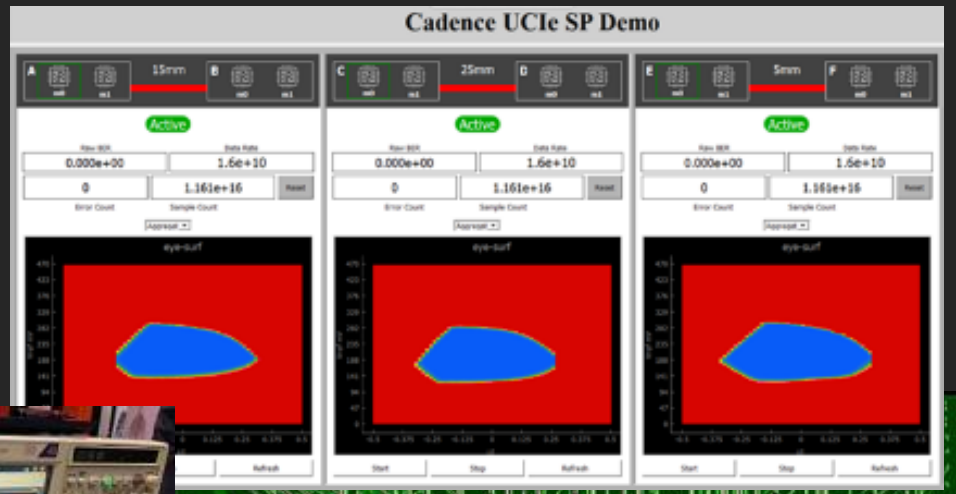
- Other Contributors:

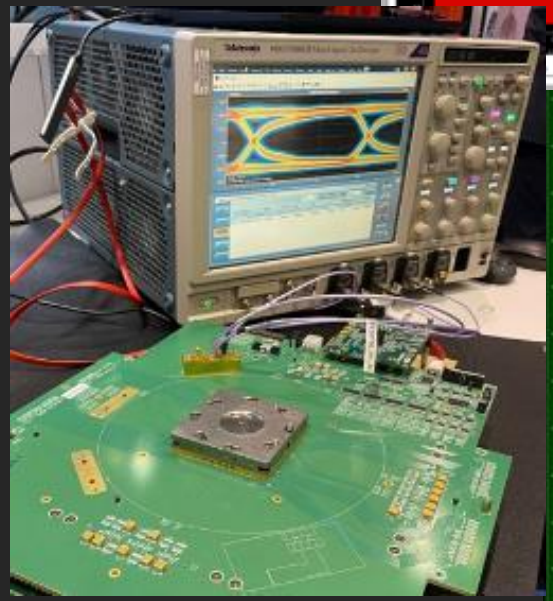
arm VENTANA xenergic

- Chiplet – leverage multiple dies in the same package
- Leverage chiplet and IP reuse
- Highlight Cadence Multi Die tools
- Utilize Samsung Multi Die Packaging

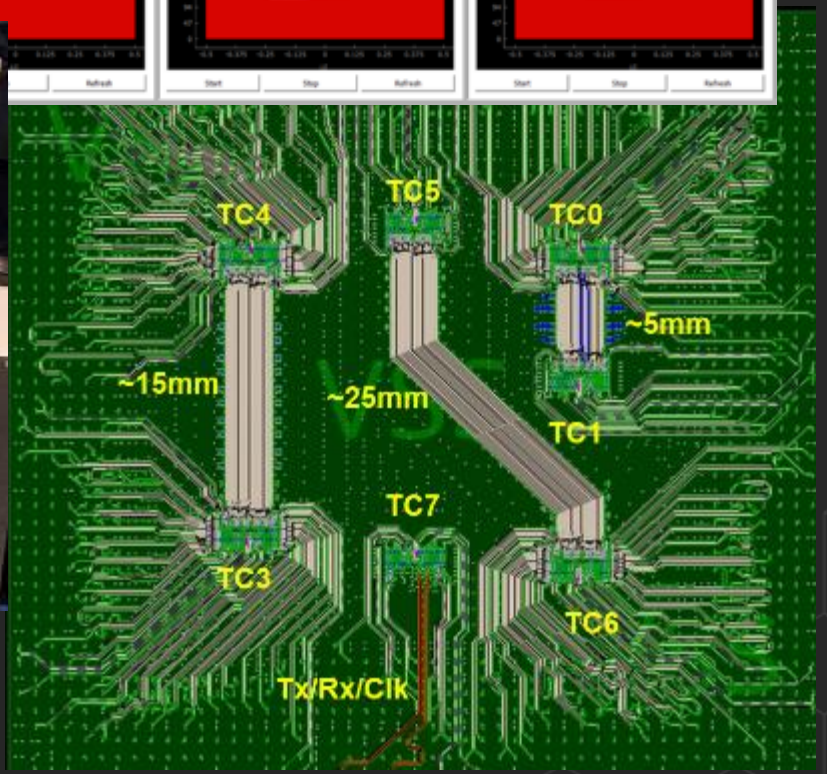
Cadence demonstrated its test chip with **seven** UCIe chiplets

- Test chip with 7 chiplets integrated into a Standard Package
- Each chiplet with 2 UCIe blocks
- 5 mm, 15 mm, and 25 mm interconnect distances
- Eye diagram and BER measurements for 16 GT/s, 12 GT/s, 8 GT/s, and 4 GT/s
- First-pass silicon success for our UCIe controller and PHY IP!



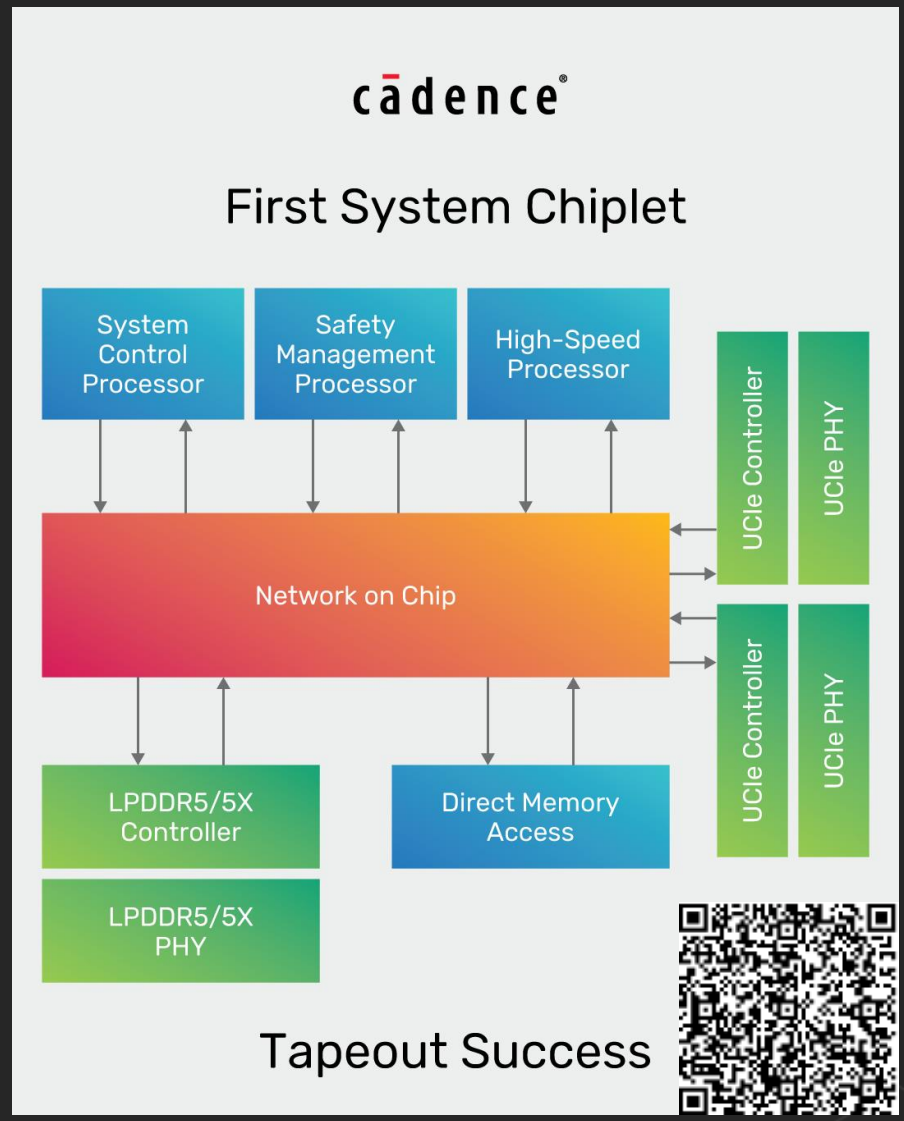


Cadence Sets the Gold Standard for UCIe Connectivity at Chiplet Summit ’24. Check out our webpage for more.



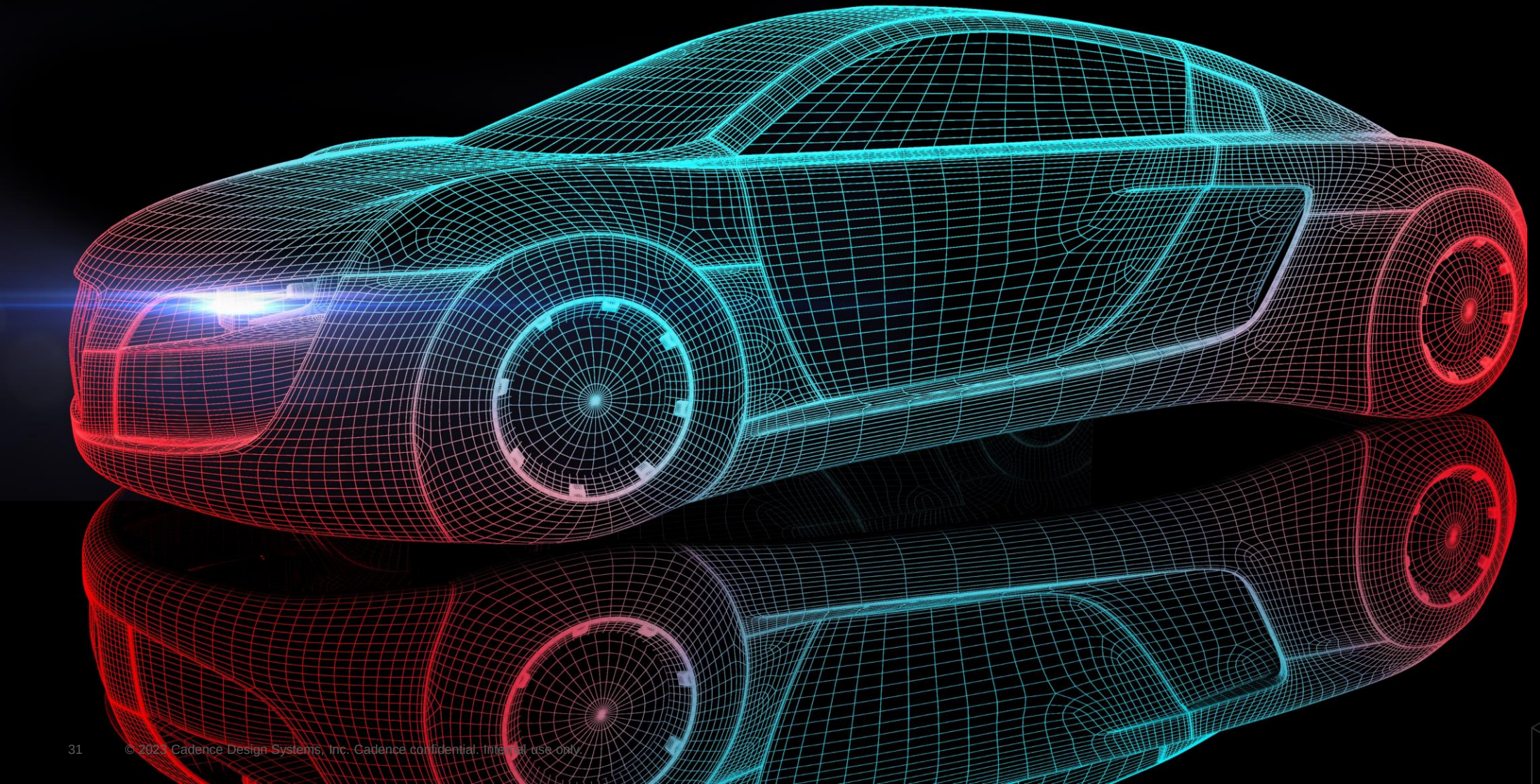
Cadence Unveils Arm-Based System Chiplet

- Cadence has announced a groundbreaking achievement with the development and successful tapeout of its first Arm-based system chiplet.
- This chiplet integrates processors, system IP, and memory IP within a single package, interconnected through the Universal Chiplet Interconnect Express™(UCIe™) standard interface.



Summary

What will cars of the future be like?

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Multi-Die Package Module
Die-1
Die-2
PCIe, CXL, Streaming
Die-to-Die Adapter
UCIe™ Main Band RX
UCIe™ Main Band TX
UCIe™ Sideband RX
UCIe™ Sideband TX
Fwd Clock, Valid, Track
x64/x16 MB Data
Fwd Clock, Valid, Track
x64/x16 MB Data
SB Data
Fwd Clock
SB Data
Fwd Clock
UCIe™ Main Band TX
UCIe™ Main Band RX
UCIe™ Sideband TX
UCIe™ Sideband RX
Die-to-Die Adapter
PCIe, CXL, Streaming
Die-to-Die Interconnect

cadence®

Let’s Connect!